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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/519,700	09/14/2005	Wade A. Krull	211843-00030	6925

27160 7590 08/05/2008

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EXAMINER	
ANGADI, MAKI A	
ART UNIT	**PAPER NUMBER**
1792	

MAIL DATE	DELIVERY MODE
08/05/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/519,700	KRULL, WADE A.	
	Examiner	Art Unit	
	MAKI A. ANGADI	1792	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 November 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. The allowability of claims 1-30 is withdrawn in view of the following rejection.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. **Claims 1-30 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.**

Claim 1 is vague and indefinite due to the terms "relatively thin", "the thickness of the first gate electrode selected to minimize gate depletion adjacent said interface" and "a heat treating temperature profile selected to minimize diffusion of said dopant at said interface".

Claim 2 is vague and indefinite due to "full thickness".

Claims 11, 17 and 19 are vague and indefinite due to the terms "relatively thin" and "the thickness of the first gate electrode selected to minimize gate depletion adjacent said interface". The metes and bounds of the above phrases are unclear.

Claim 24 is vague and indefinite due to "ultra shallow" and "shallow", especially as the preamble recites forming "an ultra shallow junction", yet the final step c) recites forming a "shallow junction".

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) The invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. **Claims 24-25 and 29-30, are rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Tokuyama et al. (US Patent No. 3,607,449).**

Tokuyama discloses a process for forming a shallow or minute junction in a semiconductor N-type silicon substrate(10) as a semiconductor device (PN junction) (Fig. 4-9, Examples 1-2, col.2, lines 44-72, col.3, lines 8-35), the process comprising the steps of: (a) depositing a dielectric layer (11)(SiO layer) on a substrate (10) (b) doping dielectric layer (col.2, lines 55-58) with boron ions at an implant energy such that the dopant is contained within the dielectric layer (col.2, lines 61-64) (c) providing heat treatment up to about 1000^{o}C to diffuse boron ions in the dielectric layer to diffuse into the substrate to form a shallow junction (col.2, lines 63-67) (claim 1).

With respect to the expression *"ultra-shallow junction"* found in the preamble of the independent claim 24, since the body of this claim only recites steps to produce a shallow junction, the expression "ultra-shallow junction" in the

preamble fails to provide any further limitation to the method claim 24. Thus, the claim is anticipated by the process for forming minute junctions (see Example 2, col.3, and line 14) as taught by Tokuyama.

Tokuyama further teaches that the penetration of the boron ions into the thin dielectric oxide layer is determined and/or controlled by the ion beam energy. See Fig. 4 and Col. 2, lines 53-64. The reference further teaches that the extent of the diffusion of the ions stored in the dielectric layer into the semiconductor substrate or the depth of the junction on the substrate is a function of the quantity of the boron ions stored in the dielectric oxide layer and the duration of the heat treatment. See col. 3 lines 63-72. Therefore, in view of the teaching of Tokuyama, it would have been obvious to one having ordinary skill in the art to use low ion beam energy for implanting a small amount of boron ions within the dielectric layer and to reduce the time of the heat treatment in order to diffuse this small amount of boron ions in the oxide dielectric layer into the substrate to finally to produce an *ultra* shallow junction in the semiconductor substrate

4. **Claims 24, 25, 27, 29 and 30 should have been rejected under 35 USC 102(b) as being anticipated by Schmitz et al., "Ultra-shallow Junction Formation by Outdiffusion from Implanted Oxide", IEEE 1988.**

Schmitz et al. teach a method for forming ultra-shallow junction in a silicon semiconductor substrate comprising depositing an oxide dielectric layer on the substrate (Fig. 1a), implanting boron ions on the substrate at a low beam

energy so that the ions are stored within the oxide dielectric layer (see Fig. 1b), and heat treating the substrate at a specified temperature and time to allow the ions within the oxide layer to diffuse into the silicon substrate to form ultra-shallow junctions on the substrate (Fig. 1c). See the whole three pages of the document, more specifically Abstract, Introduction and Fig. 1.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. **Claim 26 is rejected under 35 U.S.C. 103(a) as obvious over Tokuyama et al. (US Patent No. 3,607,449) as applied to claim 24, in further view of Lee (US Patent No. 5,777,337).**

Tokuyama discloses a single ion implant (Example 1 and 2) but is silent about series of ion implants in the fabrication of a semiconductor device. However, Lee discloses a series of ion implants i.e. boron ion implant (col.2, lines 58-61 followed by arsenic doping (col.2 lines 62-65). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement series of ion implants in the fabrication of a semiconductor device because Lee illustrates that ultra-shallow junctions can be formed by a series of ion implantation to minimize junction leakage current and to improve reliability of junction devices (col.2, lines 1-4).

6. **Claim 27 is rejected under 35 U.S.C. 103(a) over Tokuyama et al. (US Patent No. 3,607,449) as applied to claims 24 and 25 above, in further view of Mannino, *Nuclear Instruments and Methods in Physics Research B186, (2002) pages 246-255).***

Tokuyama fails to disclose doping of boron clusters in the source/drain regions. However, Mannino discloses the advantage of doping boron clusters by ion implantation in the formation of shallow junctions (page 247, col.1). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to select boron clusters for doping source/drain regions because Mannino illustrates that doping of boron clusters lead to the realization of ultra-shallow p+ source/drain structures within 100 nm from the surface (page 247).

7. **Claim 28 is rejected under 35 U.S.C. 103(a) over Tokuyama et al. (US Patent No. 3,607,449) and Lee (US Patent No. 5,777,337) as applied to claim 24 and 26 above, in further view of Marinskiy, Materials Research Society Symposium Proceedings, Vol.669, (2001), page J2.5.1-J2.5.6.**

Lee discloses doping boron into the dielectric layer but fails to disclose doping boron implant followed by hydrogen. However, Marinskiy studies the passivation of boron by hydrogen in silicon IC fabrication (page J2.5.1). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify boron doping with hydrogen because

Marinskiy illustrates the passivation of boron by hydrogen introduced into Si during typical surface treatment used in IC fabrication.

8. **Claims 24, 25, 27, 29 and 30 should have been rejected, under 35 USC 103(a) as being obvious over US patent No. 3,607,449 combined with Schmitz et al. "Ultra-shallow Junction Formation by Outdiffusion from Implanted Oxide", IEEE 1988.**

Both of the references are discussed in the anticipation rejections. One may contend that the method for forming minute junctions in a semiconductor substrate disclosed by the US '449 does not cover the formation of ultra-shallow junctions as required by the instant claims. Schmitz teaches a method for forming ultra-shallow junctions in a silicon substrate comprising similar steps in which the beam energy, annealing temperature and time for annealing are selected so that ultra-shallow junctions can be formed. It would have been obvious to one having ordinary skill in the art to modify the process of US '449 by selecting proper ion beam energy level, annealing temperature and annealing time as taught by Schmitz et al. in order to form ultra-shallow junctions on a silicon substrate.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Aronowitz (US Patent No. 5,837,598) discloses diffusion barrier for polysilicon gate electrode of MOS device.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Maki A. Angadi whose telephone number is 571-272-8213. The examiner can normally be reached on 8 AM to 4.30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine G. Norton can be reached on 571-272-1465. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Maki A Angadi/
Examiner, Art Unit 1792

/Parviz Hassanzadeh/
Supervisory Patent Examiner, Art Unit 1792